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**UNITED STATES PATENT APPLICATION**

**OF**

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**FOR**

# CARBON DOPED GaAsSb SUITABLE FOR USE IN TUNNEL JUNCTIONS OF LONG-WAVELENGTH VCSELS

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## BACKGROUND OF THE INVENTION

### Field of the Invention

**[001]** This invention relates to vertical cavity surface emitting lasers (VCSELs). More specifically, it relates to tunnel junctions for long-wavelength VCSELS.

### Discussion of the Related Art

**[002]** Vertical cavity surface emitting lasers (VCSELs) represent a relatively new class of semiconductor lasers. While there are many variations of VCSELs, one common characteristic is that they emit light perpendicular to a wafer's surface. Advantageously, VCSELs can be formed from a wide range of material systems to produce specific characteristics.

**[003]** VCSELs include semiconductor active regions, which can be fabricated from a wide range of material systems, distributed Bragg reflector (DBR) mirrors, current confinement structures, substrates, and contacts. Some VCSELs, particularly those used at long-wavelengths, incorporate tunnel junctions. Because of their complicated structure, and because of their material requirements, VCSELs are usually grown using metal-organic chemical vapor deposition (MOCVD).

**[004]** Figure 1 illustrates a typical long-wavelength VCSEL 10 having a tunnel junction. As shown, an n-doped InP substrate 12 has an n-type electrical contact 14. An n-doped lower mirror stack 16 (a DBR) is on the InP substrate 12, and an n-type graded-index InP lower spacer 18 is disposed over the lower mirror

stack 16. An InGaAsP or AlInGaAs active region 20, usually having a number of quantum wells, is formed over the InP lower spacer 18. Over the active region 20 is a tunnel junction 21. Over the tunnel junction 21 is an n-type graded-index InP top spacer 22 and an n-type InP top mirror stack 24 (another DBR), which is disposed over the InP top spacer 22. Over the top mirror stack 24 is an n-type conduction layer 9, an n-type cap layer 8, and an n-type electrical contact 26.

**[005]** Still referring to Figure 1, the lower spacer 18 and the top spacer 22 separate the lower mirror stack 16 from the top mirror stack 24 such that an optical cavity is formed. As the optical cavity is resonant at specific wavelengths, the mirror separation is controlled to resonant at a predetermined wavelength (or at a multiple thereof). At least part of the top mirror stack 24 includes an insulating region 40 that provides current confinement. The insulating region 40 is usually formed either by implanting protons into the top mirror stack 24 or by forming an oxide layer. In any event, the insulating region 40 defines a conductive annular central opening 42 that forms an electrically conductive path though the insulating region 40.

**[006]** In operation, an external bias causes an electrical current 21 to flow from the electrical contact 26 toward the electrical contact 14. The insulating region 40 and the conductive central opening 42 confine the current 21 such that the current flows through the conductive central opening 42 and into the tunnel junction 21. The tunnel junction converts incoming electrons into holes that are injected into the active region 20. Some of the injected holes are converted into photons in the active region 20. Those photons bounce back and forth (resonate) between the lower mirror stack 16 and the top mirror stack 24. While the lower mirror stack 16 and the top mirror

stack 24 are very good reflectors, some of the photons leak out as light 23 that travels along an optical path. Still referring to Figure 1, the light 23 passes through the conduction layer 9, through the cap layer 8, through an aperture 30 in electrical contact 26, and out of the surface of the vertical cavity surface emitting laser 10.

**[007]** It should be understood that Figure 1 illustrates a typical long-wavelength VCSEL having a tunnel junction, and that numerous variations are possible. For example, the dopings can be changed (say, by providing a p-type substrate), different material systems can be used, operational details can be tuned for maximum performance, and additional structures and features can be added.

**[008]** While generally successful, VCSELs similar to that illustrated in Figure 1 have problems. One problem in realizing commercial quality long wavelength VCSELs is the available mirror materials. Since long wavelength VCSELs are often based on InP, for proper lattice matching InP/InGaAsP or AlInAs/AlInGaAs mirrors are often used. However, because those materials have relatively low refractive index contrasts, 40-50 mirror pairs are typically needed to achieve the required high reflectivity. Growing that number of mirror pairs takes a long time, which increases the production costs.

**[009]** Another problem, which is addressed by the tunnel junction 21, is optical loss. In long wavelength VCSELs it is often critical to limit optical losses. To that end, p-doped materials, which absorb more light than n-doped materials, are replaced by n-doped materials and the tunnel junction 21. That junction converts holes into electrons that are injected into the active region.

**[0010]** Tunnel junctions used in semiconductor lasers are thin (say 10 nanometer), reversed biased structures. Such tunnel junctions are usually n++/p++ structures in which the p-region is highly doping (greater than $1x10^{19}$ $cm^{-3}$) using a low diffusivity dopant such as carbon. This enables a low voltage drop in a device having low free carrier absorption and sufficient free carriers.

**[0011]** Prior art semiconductor laser tunnel junctions have been reported using MBE-grown Be-doped InGaAsP or MOCVD grown C-doped AlAs. However, the reported doping in InGaAsP appears insufficient, while the strain of AlAs on InP materials appears excessive. Thus, a new long wavelength VCSEL would be beneficial. Even more beneficial would be a new tunnel junction suitable for use in long wavelength VCSELs. Still more beneficial would be new tunnel junctions that use MOCVD-grown layers and that are suitable for use in long wavelength VCSELs.

## SUMMARY OF THE INVENTION

**[0012]** Accordingly, the principles of the present invention are directed to a new tunnel junction suitable for use in long wavelength VCSELs. Beneficially, the principles of the present invention relate to MOCVD-grown tunnel junctions.

**[0013]** The principles of the present invention specifically provide for growing $GaAs_{(1-x)}Sb_x$ using MOCVD. For lattice matching with InP, x is beneficially set to 0.5 (producing a bandgap of 0.71 eV at 300K). Beneficial alternatives include setting x to 0.23, 0.3, and 0.4. During MOVCD, TMGa (or TEGa), TMSb, and $AsH_3$ (or TBAs) are used to produce the tunnel junction. Beneficially, the solid composition is controlled by controlling the ratio of As to Sb. The MOCVD growth

temperature is between 500 °C and 650 °C, while doping is beneficially performed using $CCl_4$ or $CBr_4$. The resulting p-doping can be as high as $1x10^{20}$ $cm^{-3}$ without annealing.

**[0014]** A tunnel junction according to the principles of the present invention is comprised of heavily doped $GaAs_{(1-x)}Sb_x$ and an n-doped layer of InP, AlInAs, or of a lower bandgap material such as AlInGaAs or InGaAsP. Beneficially, such a tunnel junction is formed above quantum wells to produce a VCSEL. Such VCSELs are particularly advantageous at long wavelengths.

**[0015]** Additional features and advantages of the invention will be set forth in the description that follows, and in part will be apparent from that description, or may be learned by practice of the invention.

## BRIEF DESCRIPTION OF THE DRAWING

**[0016]** The accompanying drawings, which are included to provide a further understanding of the invention and which are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention.

**[0017]** In the drawings:

**[0018]** Figure 1 illustrates a typical long-wavelength vertical cavity surface emitting laser;

**[0019]** Figure 2 illustrates a vertical cavity surface emitting laser that is in accord with the principles of the present invention;

**[0020]** Figure 3 illustrates an intermediate structure during fabrication of the vertical cavity surface emitting laser illustrated in Figure 2;

**[0021]** Figure 4 illustrates another intermediate structure during fabrication of the vertical cavity surface emitting laser illustrated in Figure 2;

**[0022]** Figure 5 illustrates yet another intermediate structure during fabrication of the vertical cavity surface emitting laser illustrated in Figure 2; and

**[0023]** Figure 6 illustrates forming the tunnel junction used in the vertical cavity surface emitting laser illustrated in Figure 2

**[0024]** Note that in the drawings that like numbers designate like elements. Additionally, for explanatory convenience the descriptions use directional signals such as up and down, top and bottom, and lower and upper. Such signals, which are derived from the relative positions of the elements illustrated in the drawings, are meant to aid the understanding of the present invention, not to limit it.

## DETAILED DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

**[0025]** The principles of the present invention are incorporated in a first embodiment VCSEL having a bottom AlGaInAs/AlInAs DBR mirror grown on an InP substrate. An example of such a VCSEL is the VCSEL 100 illustrated in Figure 2.

**[0026]** As shown in Figure 2, the VCSEL 100 includes an n-doped InP substrate 112 having an n-type electrical contact (not shown for clarity). Over the InP substrate 112 is an n-doped lower mirror stack 116 (a DBR) comprised of a plurality of alternating layers of AlGaInAs/AlInAs. Over the lower mirror stack 116 is an n-

doped InP spacer 118. The lower mirror stack 116 is beneficially grown on the InP substrate using common metal-organic and hydride sources like TMAl, TNGa, $PH_3$ and $AsH_3$ in an MOCVD process. Then, the InP spacer 118 is grown, also using MOCVD. An active region 120 comprised of P-N junction structures and having a large number of quantum wells is then formed over the InP spacer 118. The composition of the active region 120 is beneficially InGaAsP or AlInGaAs.

**[0027]** Over the active region 120 is a tunnel junction 122 comprised of a reverse biased n++/p++ junction. Beneficially, the tunnel junction includes a p-layer comprised of MOCVD-grown $GaAs_{(1-x)}Sb_x$. During MOVCD, TMGa (or TEGa), TMSb, and $AsH_3$ (or TBAs) are beneficially used to produce the $GaAs_{(1-x)}Sb_x$ layer. Beneficially, that layer's solid composition is controlled by controlling the ratio of As to Sb. The MOCVD growth temperature is between 500 °C and 650 °C. Doping is beneficially performed using $CCl_4$ or $CBr_4$ such that the resulting p-doping is greater $1x10^{19}$ $cm^{-3}$. In practice, a p-doping greater than $5x10^{19}$ $cm^{-3}$ is beneficial. It should be noted that the $GaAs_{(1-x)}Sb_x$ layer can have a doping as high as $1x10^{20}$ $cm^{-3}$ without annealing.

**[0028]** By setting x=0.5 a tunnel junction that is lattice matched to InP is produced (but $GaAs_{(.5)}Sb_{.5}$ has a bandgap of 0.71 eV at 300K). An alternative is to set x=0.4, 0.3, or 0.23, which produce $GaAs_{(1-x)}Sb_x$ layers with bandgaps of 0.8 eV, 0.91 eV, or 1eV, but which are not lattice matched to the InP active region 120. At x= 0.3, or 0.23 the strains respectively become 1.4% or 1.95%, which, while not ideal, are much better than the 3.55% strain of AlAs on InP.

**[0029]** The tunnel junction 122 further includes an n-doped layer of InP, AlInAs, or of a lower bandgap material such as AlInGaAs or InGaAsP. The n-doped layer should also be heavily doped (greater than $5x10^{19}$ $cm^{-3}$) and very thin (less than about 10 nanometers). For good lattice matching, the VCSEL 100 uses an InP n-type layer in the tunnel junction 122.

**[0030]** Over the tunnel junction 122 is an n-type InP top spacer 124. Then, an n-type top mirror structure (which includes another DBR) is disposed over the top spacer 124. The top mirror structure is beneficially comprised of a low temperature grown GaAs buffer layer 126 over the top spacer 124, a high temperature GaAs buffer layer 128 (which acts as a seed layer) over the GaAs buffer layer 126, an insulating structure (beneficially comprised of $SiO_2$) 130 over most of the GaAs buffer layer 128, and a GaAs/Al(Ga)As mirror stack 132 over the insulating structure 130. As shown, the insulating structure includes an opening 131, which enables current flow through the VCSEL 100.

**[0031]** The top mirror structure implements a device quality GaAs/Al(Ga)As mirror stack 132 over the top spacer 124. In many applications, GaAs/Al(Ga)As is considered the best material for Bragg mirrors because of its high refractive index contrast (GaAs:AlAs=3.377:2.893), high thermal conductivity (GaAs:AlAs=0.46:0.8), and its oxidation potential. However, GaAs/Al(Ga)As is seriously lattice mismatched with InP. Thus, to produce a device-quality GaAs/Al(Ga)As mirror stack, MOCVD is used in a two-step process to form intermediate GaAs buffer layers.

**[0032]** Figure 3 illustrates the first step of the two-step process. A low temperature GaAs buffer layer 126 is formed over the InP spacer 124. The low

temperature GaAs buffer layer 126 is produced by adjusting the MOCVD growth temperature to about 400-450 °C, and then MOCVD growing the low temperature GaAs buffer layer 126 to a thickness of about 20-40nm.

**[0033]** Referring now to Figure 4, after the low temperature GaAs buffer layer 126 is formed, the temperature is increased to around 600 °C. Then, the high temperature GaAs buffer layer 128 is grown. The GaAs buffer layer 128 acts as a seed layer for subsequent growths.

**[0034]** Referring now to Figure 5, after the GaAs buffer layer 128 is grown, a dielectric layer of $SiO_2$ (alternatively of $Si_3N_4$) is deposited and patterned to form the insulating structure 130. To do so, the intermediate structure shown in Figure 4 is removed from the MOCVD reactor vessel. Then, a dielectric layer of $SiO_2$ (alternatively $Si_3N_4$) is deposited on the insulating structure 130. Then, the deposited dielectric layer is patterned to produce the insulating structure 130 having the opening 131. The insulating structure 130 provides a suitable surface for lateral epitaxial overgrowth. After the insulating structure 130 formed, the intermediate structure of Figure 5 is inserted into the MOCVD reactor vessel. Referring once again to Figure 2, the GaAs/Al(Ga)As mirror stack 132 is then grown by MOCVD. That mirror stack is produced by lateral epitaxial overgrowth from the GaAs buffer layer 128 through the opening 131. The result is a high-quality mirror stack 132 having current confinement.

**[0035]** With the mirror stack 132 formed, an n-type conduction layer (similar to the p-type conduction layer 9 of Figure 1), an n-type GaAs cap layer (similar to the

p-type GaAs cap layer 8 of Figure 1), and an n-type electrical contact (similar to the p-type electrical contact 26 of Figure 1) are produced.

**[0036]** Figure 6 helps explain a method of fabricating the tunnel junction's MOCVD-grown p-doped $GaAs_{(1-x)}Sb_x$ layer. An intermediate structure 200 having an InP top surface 196 is in an MOCVD chamber 208. That chamber includes sources for Ga, Sb, and As. The Ga source 202 is beneficially either TMGa or TEGa. The Sb source 204 is beneficially TMSb, while the As source 206 is beneficially $AsH_3$ or TBAs. The composition of the $GaAs_{(1-x)}Sb_x$ layer is beneficially controlled by controlling the ratio of As to Sb. The MOCVD growth temperature is set between 500 °C and 650 °C using a thermometer 210. The doping of the $GaAs_{(1-x)}Sb_x$ layer is beneficially controlled using an atmosphere 212 containing $CCl_4$ or $CBr_4$. In practice, a p-doping greater than $5x10^{19}$ $cm^{-3}$ is beneficial. Further, while a minimum doping of $1x10^{19}$ $cm^{-3}$ is anticipated, it should be noted that the $GaAs_{(1-x)}Sb_x$ layer can have a doping as high as $1x10^{20}$ $cm^{-3}$ without annealing.

**[0037]** By setting x=0.5 a tunnel junction that is lattice matched to InP is produced (but $GaAs_{(.5)}Sb_{.5}$ has a bandgap of 0.71 eV at 300K). An alternative is to set x=0.4, 0.3, or 0.23, which produce $GaAs_{(1-x)}Sb_x$ layers with bandgaps of 0.8 eV, 0.91 eV, or 1eV, but which are not lattice matched to the InP active region 120. At x= 0.3, or 0.23 the strains respectively become 1.4% or 1.95%, which, while not ideal, are much better than the 3.55% strain of AlAs on InP. The tunnel junction 122 is further fabricated with a heavily n-doped (greater than $5x10^{19}$ $cm^3$) and very thin (less than about 10 nanometers) InP (AlInAs or of a lower bandgap material such as AlInGaAs or InGaAsP can also be used).

**[0038]** The VCSEL 100 has significant advantages over prior art long wavelength InP VCSELs. First, the two-step MOCVD process enables a device quality GaAs/Al(Ga)As top mirror to be used with an InGaAsP or AlInGaAs active region 120 and an InP top spacer 124. Another advantage is that the tunnel junction 122 enables n-doped top layers to be used, which reduces optical absorption (which can be critically important in long wavelength VCSELs). That tunnel junction 122 is comprised of a MOCVD-grown, heavily p-doped $GaAs_{(1-x)}Sb_x$ layer 198. Yet another advantage is the avoidance of InP/InGaAsP and AlInAs/AlInGaAs mirror stacks, which require larger numbers of mirror pairs. Consequently, a reduction in mirror growth times and costs is possible. Furthermore, the mirrors stacks used in the VCSEL 100 enable improved thermal performance. Still another advantage is the ease of forming current confinement in the top mirror structure, and the use of lateral epitaxial overgrowth to produce the top mirror. The overall result is a VCSEL having improved performance, increased reliability, faster fabrication, and reduced cost.

**[0039]** It will be apparent to those skilled in the art that various modifications and variation can be made in the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.